

Using Intel® Airworthiness Evidence Package (Intel® AEP) to Meet COTS Objectives of AMC/AC 20-152A

The Intel® Airworthiness Evidence Package (AEP) assists in meeting the design assurance requirements of DO-254/ED-80 and development assurance guidance of AMC/AC 20-152A for when Commercial Off The Shelf (COTS) devices are integrated into airborne electronic hardware.

Authors Introduction

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The Intel® Airworthiness Evidence Package (Intel® AEP) accelerates your time to certification by providing confidential data that is normally unavailable to customers. With access to the airworthiness-related data, Intel enables customers to build their certification packages for the full hardware and software stack. This forms the foundation for safety-critical applications. When COTS devices are integrated into airborne electronic hardware, the Intel® AEP aids in meeting the design assurance requirements of DO-254/ED-80 and the development assurance guidance of AMC/AC 20-152A.



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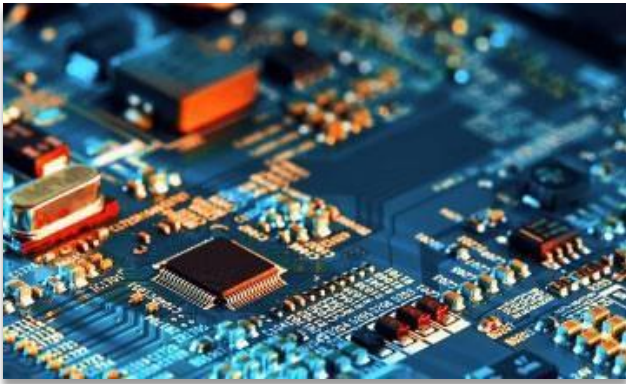
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Intel® AEP Provides Access to Flight Safety Evidence

Intel processors are built for industrial use conditions and deliver significant advantages for avionics. With their higher performance per core, Intel processors meet the needs of modern avionics subsystems while simultaneously reducing complexity with lower core counts. They scale in size, weight, performance, and cost. This provides manufacturers the ability to consolidate workloads and reduce bill of materials (BOM) costs.

Intel also designs select SKUs targeting aviation applications to meet real-time and safety-critical requirements. The critical use conditions that the processors must meet include long life of parts (7–15 years for some parts), support for extended temperature range, and high performance in a single package.

Looking across aircraft, each subsystem is categorized relative to its influence on the safe operation of the overall aircraft. The Intel® AEP provides data to help avionics manufacturers and system integrators achieve airworthiness certification ranging from DAL A through DAL D. Intel mapped functional safety evidence created to satisfy the automotive ISO 26262 and industrial IEC 61508 standards to the airborne electronic hardware DO-254 standard. The results of the mapping showed the Intel® Functional Safety Essential Design Package (Intel® FSEDP) supports customers building their own functional safety concepts.



The Intel® Airworthiness Evidence Package (Intel® AEP) further augments the Intel® FSEDP with additional evidence. This includes single event effects (SEE) analysis and interference analysis, product reliability data, product certifications, and field failure reports with the root cause analysis.

To help customers address the use of multi-core processors (MCPs) in their airborne systems, Intel provides guidance for configuring and tuning the Intel® Time Coordinated Computing (TCC) features. To enable the most predictable performance, the Intel® AEP includes a CAST-32A Guide, which provides guidance for configuring Intel processors to limit the interference between the cores and core resources.

Intel Collaborates with Avionics Systems Designers to Ensure Your Needs Are Met

We initiate each new Intel® AEP license with a kick-off meeting. In this meeting, our safety experts work with your engineering team to understand your safety-critical system, architectural block diagram, and the end-application including the I/Os and functions to be leveraged by the system.

Once agreement is reached, the silicon bill-of-materials forms the basis to help you assess the level of complexity of your selected microprocessor for the system's hardware planning document (Plan for Hardware Aspects of Certification). Working with your design team Intel collaboratively reviews this customized silicon bill of materials against the generic use cases used to develop the basic Intel® AEP. When differences are identified, Intel will review safety-related analyses to assess the impact of the deltas. The inventory of unused functions within

the processor helps you demonstrate that those unused functions do not interfere with execution of the functions being used.

Intel Provides Insight to Its Development and Change Management Processes

AMC/AC 20-152A recommends that OEMs use the electronic component management process (ECMP) defined in IEC 62239-1 ("Process management for avionics—Management plan—Part 1: Preparation and maintenance of an electronics components management plan") for selection and management of electronic components. While the standard does not apply to component manufacturers, Intel provides information to help satisfy requirements of ECMP.

Intel includes detailed information around both our silicon development process and system integration milestones in the Intel® AEP. This data provides insight into the processes Intel follows to ensure the quality of our silicon, microcode, and firmware. Intel also provides data to help with supplier selection criteria. This includes information about our conflict-free minerals policy, REACH compliance, and product discontinuation policy.

All Intel customers have access to Intel's Resource & Design Center (RDC), which provides an extensive collection of technical documentation, software, tools for designing and building with Intel products. The latest design specifications, errata sheets, and technical advisories can be accessed at any time in the RDC. Intel also maintains a dedicated site for Product Change Notifications (PCNs) and Product Discontinuance Notifications (PDNs) for products.

Potential Effects of Failures and Interference Are Identified

To meet COTS objectives, the Intel® AEP includes validation data providing confidence that parts meet published specifications. Intel performs various levels of product qualification testing before releasing its products. Intel uses dependent failure analysis (DFA) to identify the single causes that could bypass or invalidate a required independence or freedom from interference between given elements. DFA also identifies how dependent failures may affect the effectiveness of safety mechanisms, and possible countermeasures.

To understand whether safety requirements are violated due to the coexistence multiple cores within the same processor. Based on this information, Intel creates a silicon bill of materials that specifies all components within the architectural safety boundary of the system and functions, which will not be used. For elements or sub-elements with different DAL levels, Intel includes both a hardware and firmware Freedom From Interference (FFI) analysis. FFI identifies the possible source of interference between coexisting elements, which have different criticality and the possible countermeasures.



The Intel® AEP also includes a Failure Modes, Effects, and Diagnostic Analysis (FMEDA) to anticipate possible failures in the design or manufacturing process. FMEDA evaluates mitigation methods to achieve the required safety integrity. Finally this analysis calculates the safety metrics and failure rates (including soft error rates). In summary, FMEDA aims to obtain device failure rates, failure mode distribution, and diagnostic coverage of countermeasures.

Intel Processors Provide real-time and Resource Management to Improve Network Determinism

Intel real-time technology supports new solutions that require a high degree of coordination, both within and across devices. Intel® Time Coordinated Computing (Intel® TCC) enabled processors deliver optimal compute and time performance for real-time applications. Intel real-time computing performance and solutions are focused on use cases where missing a deadline could result in a system failure. Real-time offerings from Intel support new solutions that deliver both high compute and real-time performance by:

- Prioritizing real-time workloads access to cache, memory, and networking
- Minimizing disruption from other workloads
- Optimizing performance for both real-time and non-real-time workloads
- Ensuring availability in both native and virtualized environments
- Providing Intel® TCC Time Synchronization
- Providing a hardware mechanism to coordinate the various clocks found in individual IP blocks.
- Providing a hardware mechanism to specify latency of data packets from one functional block to another (Intel® TCC Timeliness).

To power complex real-time devices and support multiple systems working together in aircraft, Intel processors can pair with an Intel® Ethernet Controller featuring IEEE 802.1

time-sensitive networking (TSN) support or with any number of other networking devices. By using time synchronization and traffic scheduling, these standards enable ultra-reliable and low latency communication over Ethernet to support time sensitive applications.

Contact Info

For more information about how the Intel® AEP can help you reach your objectives, please contact us at PublicSector@intel.com

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Intel technologies may require enabled hardware, software, or service activation.

No product or component can be absolutely secure.

Your costs and results may vary.

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