

JPEG XS FPGA Evaluation Kit

High-quality, ultra-low latency, compact JPEG XS on Altera® FPGAs

The new JPEG XS ISO standard specifies a compression technology for high-quality video transport. Altera has a complete evaluation platform for this standard based on the Cyclone® 10 GX FPGA: an easy way to implement JPEG XS for your embedded video and image processing application.



Market Dynamics

Our world is changing—video is everywhere. Captured resolutions and video quality are rising, and the sheer amount of raw video data that is produced, collected, and transported is becoming unmanageable.

Transporting compressed video is becoming more popular as the market continues to see increasing demand for higher resolutions, faster frame rates, and more intelligent distribution systems.

Now more than ever, there is a need for a standardized compression solution enabling designers to manage more pixels, save cost and power, simplify connectivity, and preserve quality all with low latency and implementation complexity.

JPEG XS on Intel® FPGA responds to these challenges for custom video processing applications.

Solution in Action

JPEG XS compression can be used in applications that previously transported uncompressed image and video data—enabling systems to offer higher resolution at faster frame rates, all while retaining visually lossless quality. Target applications include:

- Live IP production, remote production
- AV over IP (SMPTE 2110 and SMPTE 2022-5/6), KVMs
- LCD and LED video walls
- Wireless displays, 5G, Internet of Things (IoT)
- LAN, WAN, cloud transmission
- Automotive, advanced driver assistance systems (ADAS)
- Omni-directional video capture systems
- Medical imaging
- Smart city cameras
- Virtual or augmented reality

Authors

Evan Pandya
Strategic Marketing
Intel Corp.

Jean-Baptiste Lorent
Director, Marketing and Sales
intoPIX

Jean-Michel Vuillamy
Technical Sales Specialist
Intel Corp.

Solution Description

Features

- Easily evaluate the quality, latency, and compression ratio of JPEG XS using a real-time encode-decode loopback
- Compact implementation suitable for edge-centric FPGAs with no need for external DDR memory
- JPEG XS (ISO/IEC 21122) is a compression technology with an end-to-end latency of a few lines.
- Complies with near-lossless quality assessment on images (ISO/IEC 29170-2)
- IntoPIX TICO-XS UHD4K 60 frames per second (fps) 444/422 encoder and decoder IP cores for JPEG XS compression are integrated with Intel HDMI 2.0 TX / RX IP on the Intel® Cyclone® 10 GX FPGA Development Kit
- Configurable codec settings allow you to evaluate different bandwidth and compression ratios
- Scalable to edge-centric FPGAs—Intel® MAX® FPGAs and Intel® Cyclone® FPGAs, including other device series—Intel® Arria®, Intel® Stratix®, and Intel® Agilex™ devices

Customer Benefits

- Low-cost way to evaluate JPEG XS in FPGA, which requires only a single Intel Cyclone 10 GX Development Kit + HDMI 2.0 FMC daughter card.
- Simple evaluation scheme requiring only one board to implement JPEG XS encode-decode loopback.
- JPEG XS IP by Intel partner intoPIX leverages the ease-of-use and productivity enabled by Intel® FPGA Video and Image Processing IP Suite (Intel® FPGA VIP IP Suite).
- Full Intel end-to-end solution: use the same JPEG-XS video codec in your embedded FPGA design using the intoPIX hardware IP and in your Intel CPU design using the intoPIX software development kit (SDK).



Learn More

- [Edge-Centric Overview Page](#)
- [HDMI Intel® FPGA IP](#)
- [Intel FPGA Video and Image Processing IP Suite](#)
- [JPEG XS](#)
- [Intel Cyclone 10 GX FPGA Development Kit](#)
- [FMC HDMI 2.0 Daughter Card – Revision 11 \(Intel OPN: FMC-HDMI-BR11-A\)](#)
- [intoPIX TICO-XS Bitstream](#)



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